AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Amended) A process for etching a silicon nitride layer with selectivity to an underlying and/or overlying dielectric layer, comprising:

introducing a semiconductor substrate into a medium density plasma etching reactor, wherein the plasma reactor comprises a dual frequency parallel plate plasma reactor having a showerhead electrode and a bottom electrode on which the substrate is supported, the bottom electrode being supplied RF energy at two different frequencies or the showerhead electrode being supplied RF energy at a first frequency and the bottom electrode being supplied RF energy at a second frequency which is greater than the first frequency, the semiconductor substrate having a layer of silicon nitride and the layer of silicon nitride having an underlying and/or overlying dielectric layer;

supplying etching gas to the plasma etching reactor and energizing the etching gas into a plasma state, the etching gas including CH_3F and at least one oxygen reactant supplied to the plasma etching reactor at a flow rate ratio of oxygen reactant to CH_3F of 0.65 to 1.5;

etching exposed portions of the silicon nitride layer with the plasma so as to etch openings in the silicon nitride layer with the plasma while providing an etch rate selectivity

of the etching rate of the silicon nitride layer to the etching rate of the dielectric layer of at least about 10.

2. (Original) The process of claim 1, wherein the dielectric layer comprises a doped or undoped silicon oxide film.

3. (Canceled)

4. (Original) The process of claim 1, wherein the etching gas is nitrogen-free.

5. (Original) The process of claim 1, wherein the etching gas consists essentially of CH_3F, oxygen and optionally Ar.

6. (Original) The process of claim 1, wherein the silicon nitride layer overlies or underlies an organic low-k dielectric material.

7. (Original) The process of claim 1, wherein the openings are 0.25 micron or smaller sized openings and/or wide open trenches.

8. (Canceled)

9. (Original) The process of clam 1, wherein the etching gas includes a carrier gas selected from the group consisting of Ar, He, Ne, Kr, Xe or mixtures thereof.

10. (Canceled)

11. (Original) The process of claim 1, wherein the etching gas is nitrogen-free and the flow rate ratio of the oxygen reactant to fluorocarbon reactant is 1 or less.

12. (Original) The process of claim 1, wherein the fluorocarbon reactant is supplied to the plasma reactor at a flow rate of 5 to 200 sccm and the oxygen reactant is supplied to the plasma reactor at a flow rate of 5 to 200 sccm.

13. (Original) The process of claim 1, further comprising applying an RF bias to the semiconductor substrate during the etching step.

14. (Original) The process of claim 1, wherein the silicon nitride layer overlies an electrically conductive or semiconductive layer comprising a metal-containing layer selected from the group consisting of doped and undoped polycrystalline or single crystal silicon, aluminum or alloy thereof, copper or alloy thereof, titanium or alloy thereof, tungsten or alloy thereof, molybdenum or alloy thereof, titanium nitride, titanium silicide, tungsten silicide, cobalt silicide, and molybdenum silicide.

15. (Original) The process of claim 1, wherein the etching step is carried out as part of a process of manufacturing a damascene structure.

16. (Original) The process of claim 1, further comprising steps of forming a photoresist layer as a masking layer, patterning the photoresist layer to form a plurality of the openings and the etching step forms via or contact openings in the silicon nitride layer.

17. (Original) The process of claim 1, wherein the silicon nitride layer is between an overlying dielectric layer and an underlying copper layer, the copper layer being exposed to the plasma in the openings during the etching step.

18. (Canceled)

19. (Original) The process of claim 1, wherein the plasma reactor is at a pressure of 5 to 1000 mTorr during the etching step.

20. (Original) The process of claim 1, wherein the semiconductor substrate comprises a silicon wafer supported on a bottom electrode and the bottom electrode is maintained at a temperature of 20 to 50° C during the etching step.

21. (Previously Presented) The process of claim 1, wherein the plasma reactor pressure is at a pressure above 80 mTorr.

22. (Previously Presented) The process of claim 1, wherein the fluorocarbon reactant is supplied to the plasma reactor at a flow rate of 20 to 40 sccm and the oxygen reactant is supplied to the plasma reactor at a flow rate of 20 to 40 sccm.

23. (Previously Presented) The process of claim 1, wherein the reactor comprises a capacitively coupled plasma reactor.